UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/908,941	07/20/2001	Masaki Hirase	010917	1043

23850 7590 11/26/2004

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/908,941	HIRASE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 12, 2004 has been entered.

Currently claims 1-10 are pending in the application. Claims 1-2 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the film" in line 15. There is insufficient antecedent basis for this limitation in the claim. Independent claim 3 does not positively recite forming “a film”.

Claim 3 recites the limitation "the first insulation " in 16. There is insufficient antecedent basis for this limitation in the claim. Independent claim 3 does not positively recite a "first insulation". The examiner believes that "the first insulation" should be replaced with –the insulation--.

Claim 9 recites the limitation "the film" in line 13. There is insufficient antecedent basis for this limitation in the claim. Independent claim 9 does not positively recite forming "a film".

Claim 9 recites the limitation "the first insulation " in 14. There is insufficient antecedent basis for this limitation in the claim. Independent claim 9 does not positively recite a "first insulation". The examiner believes that "the first insulation" should be replaced with –the insulation--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. (U.S. Patent No. 5,889,335) in view of Krivokapic et al. (U.S. Patent No. 6,087,208).

In re claim 3, Kuroi et al. disclose the method of making a semiconductor device comprising:

forming an element partitioning trench (10C) and a mask aligning trench (10A) in a semiconductor substrate (1);

simultaneously depositing an insulation (2) in the element partitioning trench and the mask aligning trench by a CVD process, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

applying a protective mask (51) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 4);

etching the insulation deposited in the mask aligning trench to remove some of the insulation (see Figure 4 and column 14, lines 37-41); and

flattening an upper surface of the semiconductor device (see column 14, lines 42-54) and selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of

forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 4, Kuroi et al. also disclose the method of forming a coating (4) on the semiconductor substrate, wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mask aligning trench and etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating (see column 14, lines 12-20).

In re claim 7, Kuroi et al. disclose the method of manufacturing a semiconductor device, comprising;

forming an silicon oxide film (3) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (4) on the silicon oxide film;

partially removing the silicon nitride film and the oxide film (see column 14, lines 12-20);

forming an element partitioning trench (10C) and a mask aligning trench (10A) by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths (see column 14, lines 12-20);

simultaneously depositing a first layer of insulation and a second layer of insulation (2A, 2C) in the element partitioning trench and in the mask aligning trench, respectively, by a CVD process, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

coating the first insulation with a protective mask (51) to fully cover the element partitioning trench (see Figure 4);

etching the second insulation so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (See Figures 4, 5 and column 14, lines 37-41);

removing the protective mask (See Figure 5 and column 14, lines 49-50); and

selectively removing the silicon nitride film and the silicon oxide film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own

admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 8, Kuroi et al. further disclose the method wherein the first insulation and the second insulation are made of the same material (2, silicon oxide).

In re claim 9, Kuroi et al. disclose the method for manufacturing a semiconductor device, the method comprising:

forming an element partitioning trench (10C) and a mask aligning trench (10A) in a semiconductor substrate (1);

simultaneously depositing an insulation (2) in the element partitioning trench and the mask aligning trench by a CVD process;

applying a protective mask (51) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 4)

etching the insulation deposited in the mask aligning trench to remove some of the insulation (see Figure 4, and column 14, lines 37-41); and

flattening an upper surface of the semiconductor device (see column 14, lines 42-54); and selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation. The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. disclose the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 10, Kuroi et al. disclose the method of manufacturing a semiconductor device, comprising;

forming an silicon oxide film (3) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (4) on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film (see column 4, lines 10-19);

forming an element partitioning trench (10C) and a mask aligning trench (10A) by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths (see column 14, lines 12-20);

simultaneously depositing a first layer of insulation and a second layer of insulation (2A, 2C) in the element partitioning trench and in the mask aligning trench, respectively, by a CVD process;

coating the first insulation with a protective mask (51) to fully cover the element partitioning trench (see Figure 4);

etching the second insulation so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (See Figures 4, 5 and column 14, lines 37-41);

removing the protective mask (See Figure 5 and column 14, lines 49-50); and

selectively removing the silicon nitride film and the silicon oxide film so that a step is formed between the upper surface of the semiconductor substrate and an upper

surface of the first insulation (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. (U.S. Patent No. 5,889,335) and Krivokapic et al. (U.S. Patent No. 6,087,208) in view of Schoenfeld (U.S. Patent No. 6,127,245).

In re claim 5, Kuroi et al. and Krivokapic et al. disclose the method as claimed and rejected above including the steps of flattening by a chemical mechanical process, wherein the coating functions as a stopper, but do not disclose that the method of flattening is performed rotary grinding. Schoenfeld discloses the method of utilizing a rotary grinder in CMP process (see column 5, lines 30-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rotary grinding disc in the CMP process of the combined Kuroi et al. and Krivokapic et al. in order to create a uniform flat surface that allows for ease of formation of subsequently formed devices.

In re claim 6, Kuroi et al. disclose the method wherein the semiconductor substrate is a silicon substrate (1) the insulation is formed from silicon oxide (2), the coating is formed from silicon nitride (4); the method further comprising the step of forming a silicon oxide film (3) on the semiconductor substrate prior to the formation of the element partitioning trench and the mask aligning trench, wherein the coating is formed on the silicon oxide film (see Figure 2-3).

Response to Arguments

Applicant's arguments with respect to claims 3-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al. (Silicon Processing for the VLSI Era, Volume 1-Process Technology, 1986, Lattice Press, page 1) discloses the advantages to silicon substrates and silicon oxide.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk